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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,734	12/30/2003	Yibin Ye	110350-134110	9041

31817 7590 10/24/2005

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,734	YE ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,11-17 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11-17 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 10/10/2005 has been entered.

2. Claims 1-3, 11-17,21-23 are presented for examination.

Drawings

3. The drawings were received on 10/10/2005. This drawing is Figure 5.

Response to Arguments

4. Applicant's arguments with respect to claims 1-3, 11-17,21-23 have been considered but are moot in view of the new ground(s) of rejection.

Double Patenting

5. Claim 13 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 12. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Regarding claims 12-13, they are both cover the same invention.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 11-17,21-23 are rejected under 35 U.S.C. 102(b) as being **clearly anticipated** by Noble (U.S. Patent No. 6,246,083).

Regarding claim 1, Noble discloses a two-transistor DRAM cell (Figure 2) consisting:

An NMOS device (26) with a first gate (65, Column 6, lines 10-15);

A PMOS device (28, Column 6, lines 10-15) with a second gate, the PMOS device coupled to the NMOS device (Figure 2); and

A storage node (110) coupled to the second gate (Figure 2, Column 6, lines 20).

Regarding claims 2-3, Noble discloses wherein the storage node is defined the PMOS device and the NMOS device, the storage node having a voltage that converges to Vhigh, where Vhigh is greater than Vcc/2 (Column 7, lines 20-44), and the PMOS device (28) is coupled between the read bit line (90) and the read word line (95); and the NMOS device is coupled to the PMOS device so as to defined a storage node therebetween (Figures 2-3).

Regarding claims 11-17, 21-23, Noble disclose a two-transistor DRAM cell (Figure 2) consisting:

A read bit line (RBL);

A write bit line (WBL);

A read word line (RWL);

A write word line (WWL);

A p-channel device (28) coupled between the read bit line and the read word line (Figure 2); and an n-channel device (26) coupled between the write bit line and a gate region of the PMPS device so as to form a storage node therebetween (110). More specifically, Noble discloses wherein the NMOS device comprises a gate region (Figure 2, 65) coupled to the write word line (WWL), and wherein the NMOS device is coupled to the write word line, and wherein the write word line is pulled from a logic low voltage to a logic high voltage to write data into the DRAM cell (Column 7, lines 20-25), and wherein the read word line, the read bit line and write word line are held at a logic low voltage to hold data within the DRAM cell (Column 7, lines 45-47), and wherein the data written into the DRAM cell corresponds to the voltage level of the write bit lien (Column 7, lines 25-27), and wherein a voltage level of the storage node converges to logic due to edge leakage current (Column 7, lines 27-29), and a system comprising an integrated circuit (Column 1, lines 11-15).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827